23.3 An ESD-Protected DC-to-6GHz 9.7mW LNA in 90nm Digital CMOS

J. Borremans[1,2], P. Wambacq[1,2], D. Linten[1,2]

[1]IMEC, Leuven, Belgium
[2]Vrije Universiteit Brussel, Brussels, Belgium

The high f_t of scaled CMOS transistors enables lots of design freedom in the low-GHz frequency range at the price of increasingly expensive silicon area, certainly when on-chip inductors are needed to achieve the required performance. Therefore, some of the RF performance should be invested in lowering power consumption and area usage. Inductorless feedback-type LNAs are an excellent illustration of this fact, receiving a lot of attention throughout the past years [1-3]. In this paper, a low-cost low-area (50×35μm²) low-power (9.8mW) DC-to-6GHz LNA solution in 90nm digital CMOS is presented. ESD protection (3.2kV HBM) is implemented, as well as an optional second stage with gain selection.

High-performance wideband low-area inductorless topologies, such as noise-cancelling LNAs [2] or feedback-type designs [1,3] suffer from high power, limited bandwidth, or inadequate NF. Scaling CMOS towards 90nm and beyond however, allows efficient feedback LNA design. As shown in [4], most feedback-type solutions are comparably promising. In this work, a shunt-shunt feedback-type solution is proposed, as is illustrated by the first stage of the circuit in Fig. 23.3.1. Its simple structure inherently could use only transistors, and is thus is appealing for any digital technology. Additionally, the simplicity is favorable, since a low number of components introduce less parasitics.

The amplifier is designed as a single-stage and a two-stage version (Fig. 23.3.1) in a digital 90nm CMOS process. A cascode stage M_{n1}-M_{nCasc} offers gain while the feedback via source-follower M_{n2} ensures input matching, maintaining a low NF. To increase design freedom and reduce the dependency of the gain and matching on the output conductance at node A, the load is constructed by a transistor in parallel with a resistor R_{load} (n-type diffusion). As no capacitors are required, the circuit is naturally broadband from DC to its bandwidth, and uses negligible silicon area. Furthermore, DC stability is guaranteed by the negative feedback. The voltage gain is given by $A_V = g_{mMn1}.R_L$, where $g_{mMn1} \approx$ 80mS, and R_L is the total load impedance at node A. Input matching is achieved when

$$g_{mMn2} = \frac{1}{R_S \cdot (1 + g_{mMn1} \cdot R_L)}, \quad (1)$$

where R_S is the input port impedance (50Ω). The noise figure for the first stage under matching conditions is:

$$F \approx 1 + \frac{\gamma_1}{g_{mMn1} \cdot R_S} + \frac{\gamma_2}{1 + g_{mMn1} \cdot R_L} + \frac{1}{g_{mMn1}^2 \cdot R_L \cdot R_S} + \frac{R_S}{R_{Bias}}, \quad (2)$$

where R_{Bias} is the output resistance of the bias transistor M_{nBias}, and $\gamma_{1,2}$ are the noise excess factors of the transistors M_{n1} and M_{n2}, respectively. Clearly, a large g_m is required for M_{n1} to lower the NF. The scaled CMOS allows transistor M_{n1} to operate in moderate inversion, lowering power consumption significantly for a large g_{mMn1} and maintaining a reasonable bandwidth.

Linearity is mainly limited by the nonlinear feedback via M_{n2}. Indeed, the signal swing is the largest at the circuit output which is the gate of M_{n2}. As a consequence, M_{n2} generates significant second-order distortion at the circuit input, which propagates linearly to the output. The second-order nonlinearity of M_{n2} combines this second-order distortion with the fundamental of the output signal of the circuit, producing third-order distortion at the circuit input. Finally, this third-order distortion propagates linearly to the output. The IIP3 of the LNA taking only into account the dominant contribution of M_{n2}, is approximately given by:

$$IIP3 \approx \frac{4}{1 + A_V} \sqrt{\frac{2}{3\left[\left(\frac{K_{2gmMn2}}{g_{mMn2}}\right)^2 + \frac{K_{3gmMn2}}{g_{mMn2}}\right]}}, \quad (3)$$

where K_{2gmMn2} and K_{3gmMn2} are the slope and the curvature of g_m as a function of v_{GS} [5]. These coefficients decrease drastically when the inversion level increases. Thus, linearity can be increased significantly by moderately increasing the inversion level of M_{n2}.

An optional cascode second stage introduces gain selection with transistor M_{pGS}. Gain selection in an LNA is often needed to avoid overdriving a possible subsequent mixer. Providing that functionality in the second stage preserves input matching and a fairly low NF. Capacitor C_{dec} (MoM–capacitor) ensures AC ground at the source of M_{nSS1}, while R_{SS1} allows the selection of an appropriate overdrive for M_{nSS1}. A common-source buffer drives the 50Ω for the purpose of measurement in both amplifier configurations.

Figures 23.3.2 and 23.3.3 present gain, NF, matching and linearity for the LNAs. A minimum NF of 2.5dB is attainable for 9.8mW at a low power supply of 1.2V. The bandwidth (defined as the minimum of the input matching bandwidth (S_{11}<–10dB) and the 3dB S_{21} bandwidth) makes this LNA suitable for DC-to-6GHz operation. Possible applications are 3-to-5GHz UWB or multi-standard receivers. The second stage adds about 4dB to the 17dB gain of the first stage (Fig. 23.3.4) while it draws 3mA extra from the supply. Even for the low gain mode the NF is still fairly low (5dB). Allowing only minor NF degradation, the LNA can be operated at very low power (3.4mW) at a lowered supply of 1V (Fig. 23.3.5). At this power, no significant bandwidth reduction is observed.

ESD protection is of great importance in scaled CMOS technologies, as the gate oxide breakdown voltage is as low as 4.1V in 90nm. For low area and wideband ESD protection, STI diodes have been selected since they moderately stress the attainable bandwidth and NF. On-wafer HBM tests show an excellent protection level of 3.5kV (positive to V_{DD}) and 3.2kV (negative to ground) HBM. This corresponds to the failure level measured for the standalone diodes. Minor degradation is noted in performance due to careful selection of the diode size (19.5×1.5μm²) (Fig. 23.3.2).

A micrograph of the circuit (Fig. 23.3.7) shows the low active area (50×35μm²), smaller than a bond pad. This is quite natural for the single-stage version, since no capacitors are used at all. This work offers a low-cost efficient low-power low-area LNA solution that is suitable for digital scaled CMOS technologies. Figure 23.3.6 shows a comparison between the results achieved by recently published circuits. Power consumption is seven times lower than in [1], for a supply voltage of 1.2V using only standard digital devices in a 90 nm process.

Acknowledgement:
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References:
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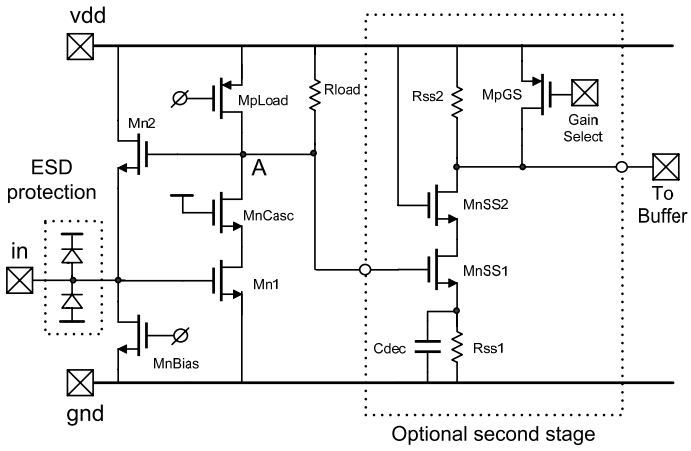

Figure 23.3.1: The LNA schematic with optional second stage and ESD protection.

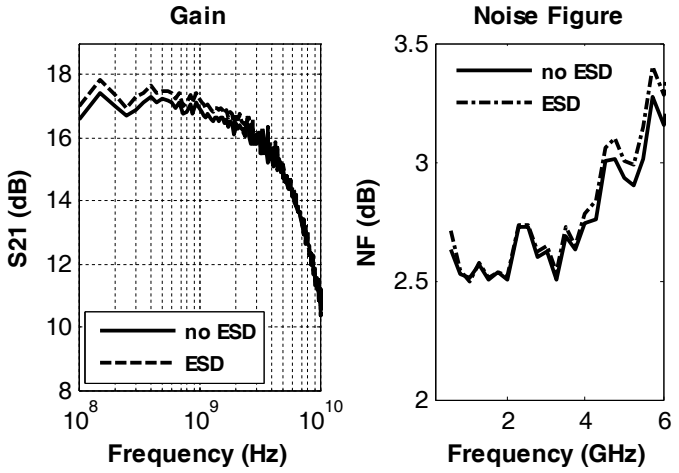

Figure 23.3.2: Power Gain (S_{21}) and NF of the one-stage LNA.

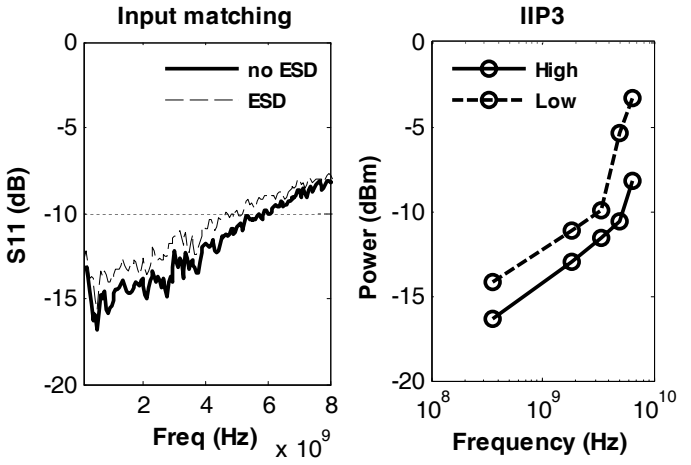

Figure 23.3.3: Input matching and IIP3.

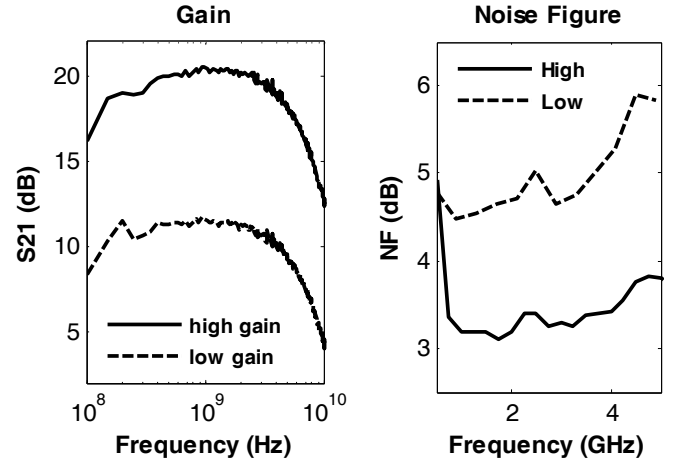

Figure 23.3.4: Gain and NF of the two-stage LNA.

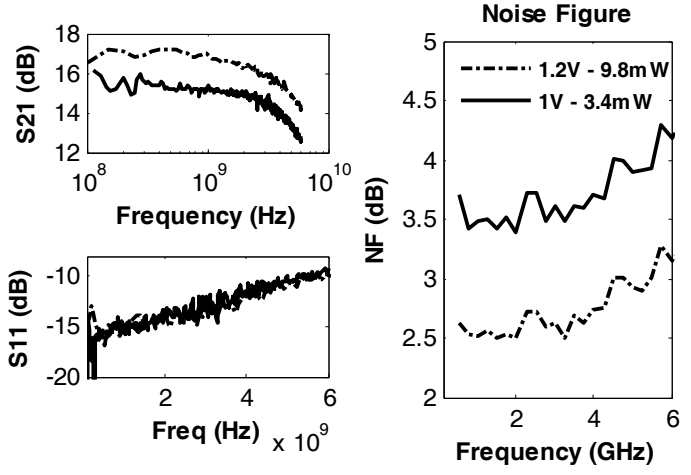

Figure 23.3.5: Lowering V_{DD} to reduce power consumption.

Source	Tech-nology	Freq (*) (GHz)	Gain (dB)	NFmin (dB)	Power (mW)	V_{DD} (V)	Area (mm^2)	FOM (dB)
This work Single Stage	Dig. 90nm CMOS	0-6	15.3	3.4	**3.4**	1	**0.0017**	**18.7**
This work Single Stage	Dig. 90nm CMOS	0-6	17.4	2.5	**9.8**	1.2	**0.0017**	**15.3**
[Zhan] ISSCC2006 [1]	RF 90nm CMOS	0.5-6	25	2	42	2.7	~0.025	12.0
[Cherazhi] CICC2005	0.13um CMOS	0.4-6.5	18	3	11.7	1.8	~0.4	12.4
[Wang] RFIC 2005 [3]	0.13um CMOS	0.1-0.9	13	4	0.7	1.2	**	10.9
[Heydari] RFIC 2005	0.18um CMOS	0.1-11	8	2.9	21.6	1.8	~0.3	2.5
[Blaakmeer] RFIC 2006	90nm RF CMOS	2.5-4	19	4	8	1.2	~0.2	0.9
[Bruccoleri] JSSC2004 [2]	0.25um CMOS	0.15-1.8	13.7	1.9	35	2.5	~0.075	-7.6

$$FOM = 20 \cdot \log_{10}\left(\frac{Gain[lin] \cdot BW[GHz]}{Power_{DC}[mW] \cdot (NF[lin]-1)}\right)$$

(* minimum of 3 dB bandwidth and S_{11} < -10dB, ** unknown)

Figure 23.3.6: Performance summary and comparison.

Continued on Page 613

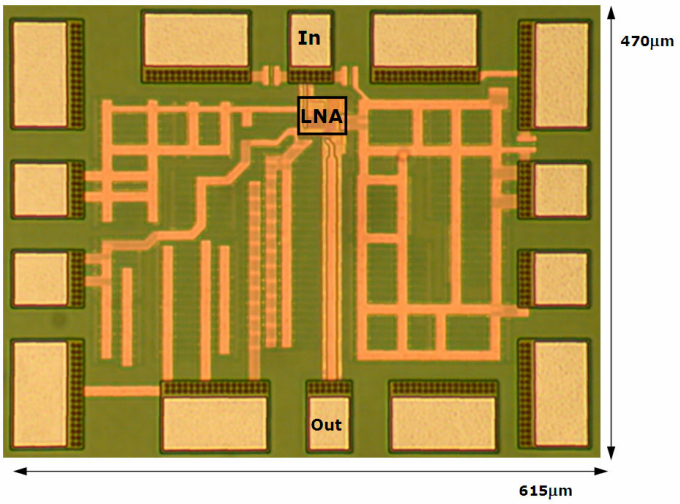

Figure 23.3.7: Chip micrograph of the ESD-protected 1-stage LNA

